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R. Peset Llopis
December 1995 **Proceedings of the conference on European design automation**
Full text available: pdf(672.15 KB) Additional Information: full citation, references, index terms

2 Provably correct high-level timing analysis without path sensitization
Subhrajit Bhattacharya, Sujit Dey, Franc Brglez
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(820.65 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper addresses the problem of true delay estimation during high level design. The existing delay estimation techniques either estimate the topological delay of the circuit which may be pessimistic, or use gate-level timing analysis for calculating the true delay, which may be prohibitively expensive.We show that the paths in the implementation of a behavioral specification can be partitioned into two sets, SP and UP. While the paths in SP can affect the delay of the circuit ...

3 VIPER: an efficient vigorously sensitizable path extractor
Hoon Chang, Jacob A. Abraham
July 1993 **Proceedings of the 30th international conference on Design automation**
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4 Incremental techniques for the identification of statically sensitizable critical paths
Yun-Cheng Ju, Resve A. Saleh
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
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5 Dynamic search-space pruning techniques in path sensitization
João P. Marques Silva, Karem A. Sakallah
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(80.72 KB) Additional Information: full citation, references, citings, index terms

6 A single-path-oriented fault-effect propagation in digital circuits considering multiple-path sensitization

M. Henftling, H. C. Wittmann, K. J. Antreich

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(103.72 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Various satisfiability problems in combinational logic blocks as, for example, test pattern generation, verification, and netlist optimization, can be solved efficiently by exploiting the fundamental concepts of propagation and justification. Therefore, fault effect propagation gains further importance. For the first time, we provide the theoretical background for a single path oriented fault effect propagation considering both single and multiple path sensitization. We call this approach SPOP. ...

Keywords: ATPG, test generation, propagation

7 Exact path sensitization in timing analysis

R. Peset Llopis

September 1994 **Proceedings of the conference on European design automation**

Full text available: pdf(636.19 KB) Additional Information: full citation, references, citings, index terms

8 Delay test and BIST: TranGen: a SAT-based ATPG for path-oriented transition faults

Kai Yang, Kwang-Ting Cheng, Li-C. Wang

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Full text available: pdf(118.88 KB) Publisher Site Additional Information: full citation, abstract, references

This paper presents a SAT-based ATPG tool targeting on a path-oriented transition fault model. Under this fault model, a transition fault is detected through the longest sensitizable path. In the ATPG process, we utilize an efficient false-path pruning technique to identify the longest sensitizable path through each fault site. We demonstrate that our new SAT-based ATPG can be orders-of-magnitude faster than a commercial ATPG tool. To demonstrate the quality of the tests generated by our approac ...

9 Test generation for primitive path delay faults in combinational circuits

Ramesh C. Tekumalla, Prem R. Menon

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(77.69 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a method of identifying primitive path-delay faults in combinational circuits, and deriving robust tests for all robustly testable primitive faults. It uses the concept of sensitizing cubes to reduce the search space. This approach helps identify faults that cannot be part of any primitive fault, and avoids attempting test generation for them. Sensitization conditions determined for primitive fault identification are also used in test generation, reducing test generation effo ...

Keywords: Sensitizing cubes, static sensitizability, primitive faults, test generation

10 Timing analysis based on primitive path delay fault identification
Mukund Sivaraman, Andrzej J. Strojwas
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(55.35 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We present a novel timing analysis mechanism which is based on identifying primitive path delay faults (primitive PDFs) in a circuit. We show that this approach gives the exact maximum delay of the circuit under the floating mode of operation assumption. Our timing analysis approach provides a framework where component delay correlations and signal correlations arising from fabrication process, signal propagation, and signal interaction effects can be handled very accurately. Under these effects ...

Keywords: timing analysis, false path, timing verification, path delay fault testing, primitive path delay faults, correlated delay, floating mode

11 Performance optimization using exact sensitization
Alexander Saldanha, Heather Harkness, Patrick C. McGeer, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli
June 1994 **Proceedings of the 31st annual conference on Design automation**
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12 Dynamical identification of critical paths for iterative gate sizing
How-Rern Lin, TingTing Hwang
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(514.60 KB) Additional Information: full citation, abstract, references, index terms

Since only sensitizable paths contribute to the delay of a circuit, false paths must be excluded in optimizing the delay of the circuit. Just identifying false paths in the first place is not sufficient since during iterative optimization process, false paths may become sensitizable, and sensitizable paths false. In this paper, we examine cases for false path becoming sensitizable and sensitizable becoming false. Based on these conditions, we adopt a so-called loose sensitization criterion ...

13 An efficient parallel critical path algorithm
Li-Ren Liu, David H. C. Du, Hsi-Chuan Chen
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
Full text available: pdf(772.96 KB) Additional Information: full citation, references, citings, index terms

14 Efficient algorithms for computing the longest viable path in a combinational network
P. C. McGeer, R. K. Brayton
June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**
Full text available: pdf(906.35 KB) Additional Information: full citation, abstract, references, citings, index terms

We consider the elimination of false paths in combinational circuits. We give the single generic algorithm that is used to solve this problem, and demonstrate that it is parameterized by a Boolean function called the sensitization condition. We give two criteria which we argue that a valid sensitization condition must meet, and introduce four conditions that have appeared in the recent literature, of which two meet the criteria and two do not. We then introduce a dynamic pr ...

15 Timing abstraction: An implication-based method to detect multi-cycle paths in large sequential circuits
Hiroyuki Higuchi
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(247.01 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper proposes a fast multi-cycle path analysis method for large sequential circuits. It determines whether or not all the paths between every flip-flop pair are multi-cycle paths. The proposed method is based on ATPG techniques, especially on implication techniques, to utilize circuit structure and multi-cycle path condition directly. The method also checks whether or not the multi-cycle path may be invalidated by static hazards in combinational logic parts. Experimental results show that ...

Keywords: ATPG, implication, multi-cycle path, sequential circuits

16 DynaTAPP: dynamic timing analysis with partial path activation in sequential circuits
Prathima Agrawal, Vishwani D. Agrawal, Sharad C. Seth
November 1992 **Proceedings of the conference on European design automation**

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17 RESIST: a recursive test pattern generation algorithm for path delay faults
Karl Fuchs, Michael Pabst, Torsten Rössel
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18 The role of long and short paths in circuit performance optimization
S. W. Cheng, H.-C. Chen, D. H. C. Du, A. Lim
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

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19 Advances in timing and simulation: False-path-aware statistical timing analysis and efficient path selection for delay testing and timing validation
Jing-Jia Liou, Angela Krstic, Li-C. Wang, Kwang-Ting Cheng
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(77.58 KB) Additional Information: full citation, abstract, references, citings, index terms

We propose a false-path-aware statistical timing analysis framework. In our framework, cell as well as interconnect delays are assumed to be correlated random variables. Our tool can characterize statistical circuit delay distribution for the entire circuit and produce a set of true critical paths.

Keywords: critical path selection, false path, statistical timing analysis

20 Generation of high quality non-robust tests for path delay faults
Kwang-Ting Cheng, Hsi-Chuan Chen
June 1994 **Proceedings of the 31st annual conference on Design automation**

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Hiroyuki Higuchi
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This paper proposes a fast multi-cycle path analysis method for large sequential circuits. It determines whether or not all the paths between every flip-flop pair are multi-cycle paths. The proposed method is based on ATPG techniques, especially on implication techniques, to utilize circuit structure and multi-cycle path condition directly. The method also checks whether or not the multi-cycle path may be invalidated by static hazards in combinational logic parts. Experimental results show that ...

Keywords: ATPG, implication, multi-cycle path, sequential circuits

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June 1994 **Proceedings of the 31st annual conference on Design automation**
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3 Elimination of multi-cycle false paths by state encoding
Z. Hasan, M. J. Ciesielski
March 1995 **Proceedings of the 1995 European conference on Design and Test**
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In this paper we present a technique to remove multi-cycle false paths from a sequential circuit by the encoding of its states. Based on behavioral level analysis, we derive the necessary and sufficient condition for the encoding of FSM to obtain a false path free implementation. This condition requires the satisfaction of false path dichotomies obtained from symbolic output and next state equations of the machine. The presented approach can significantly impact the multi-cycle false path remova ...

Keywords: FSM encoding, behavioral level analysis, encoding, finite state machines, logic design, multi-cycle false paths elimination, sequential circuit synthesis, sequential circuits, sequential switching, state encoding

4 Exploiting multi-cycle false paths in the performance optimization of sequential circuits
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5 Path sensitization of combinational circuits and its impact on clocking of sequential systems
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6 Automated multi-cycle symbolic timing verification of microprocessor-based designs
Anurag P. Gupta, Daniel P. Siewiorek
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(140.84 KB) Additional Information: full citation, references, citings, index terms

7 Waiting false path analysis of sequential logic circuits for performance optimization
Kazuhiro Nakamura, Kazuyoshi Takagi, Shinji Kimura, Katsumasa Watanabe
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
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8 Provably correct high-level timing analysis without path sensitization
Subhrajit Bhattacharya, Sujit Dey, Franc Brglez
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(820.65 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper addresses the problem of true delay estimation during high level design. The existing delay estimation techniques either estimate the topological delay of the circuit which may be pessimistic, or use gate-level timing analysis for calculating the true delay, which may be prohibitively expensive.We show that the paths in the implementation of a behavioral specification can be partitioned into two sets, SP and UP. While the paths in SP can affect the delay of the circuit ...

9 Practical issues in logic synthesis: Enhancing the performance of multi-cycle path analysis in an industrial setting
Hiroyuki Higuchi, Yusuke Matsunaga
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**
Full text available: pdf(117.87 KB) Publisher Site Additional Information: full citation, abstract, references

In this paper we enhance the performance of multi-cycle path analysis in an industrial setting. Industrial designs are, in general, more complicated, but contain more information

than fundamental sequential circuits. We show how such information is used for improving the quality and the efficiency of multi-cycle path analysis. Specifically, we propose local FSM learning to take into account reachability information. We also propose **FF** enable learning to accelerate multi-cycle path analysi ...

10 VIPER: an efficient vigorously sensitizable path extractor
Hoon Chang, Jacob A. Abraham
July 1993 **Proceedings of the 30th international conference on Design automation**
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11 Incremental techniques for the identification of statically sensitizable critical paths
Yun-Cheng Ju, Resve A. Saleh
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
Full text available: pdf(683.79 KB) Additional Information: full citation, references, citings, index terms

12 Session S3.1: architecture adaptation and synthesis: Cycle-time aware architecture synthesis of custom hardware accelerators
Mukund Sivaraman, Shail Aditya
October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(75.23 KB) Additional Information: full citation, abstract, references, index terms

We present the cycle-time aware architecture synthesis methodology used in PICO-NPA that automatically synthesizes minimal cost RT-level designs from high-level specifications to meet a given cycle-time. This allows subsequent physical synthesis to succeed on first pass with predictable performance. The core of the methodology is a static timing analysis engine that is used at multiple levels - program-level, architecture-level and RT-level - in order to identify, schedule and validate useful op ...

Keywords: clock frequency, delay analysis, embedded hardware architecture synthesis, high-level synthesis, operator chaining, target clock period, timing analysis, timing during scheduling

13 Exact minimum cycle times for finite state machines
William K. C. Lam, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(142.50 KB) Additional Information: full citation, references, index terms

14 Full chip false timing path identification: applications to the PowerPCTM microprocessors
J. Zeng, M. Abadir, J. Bhadra, J. Abraham
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
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15 Test point insertion: scan paths through combinational logic
Chih-chang Lin, Malgorzata Marek-Sadowska, Kwang-Ting Cheng, Mike Tien-Chien Lee
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(323.60 KB) Additional Information: full citation, references, citings, index terms

16 Oscillation control in logic simulation using dynamic dominance graphs
Peter Dahlgren
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(125.57 KB) Additional Information: full citation, references, index terms

17 Complexity of sequential ATPG
T. E. Marchok, A. El-Maleh, W. Maly, J. Rajski
March 1995 **Proceedings of the 1995 European conference on Design and Test**
Full text available: pdf(1.20 MB) Additional Information: full citation, abstract, citings
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The research reported in this paper was conducted to identify those attributes, of both sequential circuits and structural, sequential automatic test pattern generation (ATPG) algorithms, which can lead to extremely high test generation times. The retiming transformation is used as a mechanism to create two classes of circuits which present varying degrees of complexity for test generation. It was observed for three different sequential test generators that the increase in complexity of testing ...

Keywords: VLSI, automatic test pattern generation, automatic testing, circuit attribute, density of encoding, design for testability, integrated circuit testing, logic testing, retiming transformation, sequential ATPG, sequential circuits, structural ATPG, test generation times, testing complexity, timing

18 Timing verification and the timing analysis program
R. B. Hitchcock
June 1988 **Papers on Twenty-five years of electronic design automation**
Full text available: pdf(1.19 MB) Additional Information: full citation, references, citings, index terms

19 A heuristic covering technique for optimizing average-case delay in the technology mapping of asynchronous burst-mode circuits
P. Beerel, W. Chou, K. Yun
September 1996 **Proceedings of the conference on European design automation**
Full text available: pdf(354.20 KB) Additional Information: full citation, references, index terms

20 Advances in timing and simulation: False timing path identification using ATPG techniques and delay-based information
Jing Zeng, Magdy Abadir, Jacob Abraham
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(112.25 KB) Additional Information: full citation, abstract, references, index terms

A well-known problem in timing verification of VLSI circuits using static timing analysis tools is the generation of false timing paths. This leads to a pessimistic estimation of the processor speed and wasted engineering effort spent optimizing unsensitizable paths. Earlier results have shown how ATPG techniques can be used to identify false paths efficiently [6],[9], as well as how to bridge the gap between the physical design on which the static timing analysis is based and the test view on w ...

Keywords: ATPG, false timing paths, static timing analysis, timing slack

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1 Efficient circuit partitioning to extend cycle simulation beyond synchronous circuits
Charles J. DeVane
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(194.27 KB) Additional Information: full citation, abstract, references, citings, index terms
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Cycle simulation techniques, such as levelized compiled code, can ordinarily be applied only to synchronous designs. They usually cannot be applied to designs containing circuit features like combinational paths, multiple clock domains, generated clocks, asynchronous resets, and transparent latches. This paper presents a novel partitioning algorithm that partitions a non-cycle-simulatable circuit containing these features into sub-circuits that can be cycle simulated. Cycle simulation techniques ...

Keywords: logic simulation, cycle simulation, circuit partitioning, levelized compiled code

2 Evaluating the accuracy of defect estimation models based on inspection data from two inspection cycles
Stefan Biffl, Wilfried Grossmann
July 2001 **Proceedings of the 23rd International Conference on Software Engineering**
Full text available: pdf(182.59 KB) Additional Information: full citation, abstract, references, citings, index terms
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Defect content estimation techniques (DCETs), based on defect data from inspection, estimate the total number of defects in a document to evaluate the development process. For inspections that yield few data points DCETs reportedly underestimate the number of defects. If there is a second inspection cycle, the additional defect data is expected to increase estimation accuracy.

In this paper we consider 3 scenarios to combine data sets from the inspection-reinspection process ...

3 Exact minimum cycle times for finite state machines
William K. C. Lam, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(142.50 KB) Additional Information: full citation, references, index terms

4

Strongly polynomial-time and NC algorithms for detecting cycles in periodic graphs
Edith Cohen, Nimrod Megiddo
September 1993 **Journal of the ACM (JACM)**, Volume 40 Issue 4
Full text available: pdf(2.88 MB) Additional Information: full citation, references, citings, index terms, review

Keywords: application of multidimensional search, application of parametric method, strongly polynomial algorithms periodic graphs

5 Cyclic and non-cyclic combinational circuit synthesis: The synthesis of cyclic combinational circuits
Marc D. Riedel, Jehoshua Bruck
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(174.99 KB) Additional Information: full citation, abstract, references, citings, index terms

Digital circuits are called combinational if they are memoryless: they have outputs that depend only on the current values of the inputs. Combinational circuits are generally thought of as acyclic (i.e., feed-forward) structures. And yet, cyclic circuits can be combinational. Cycles sometimes occur in designs synthesized from high-level descriptions. Feedback in such cases is carefully contrived, typically occurring when functional units are connected in a cyclic topology. Although the premise o ...

Keywords: combinational logic, cycles, feedback, logic synthesis

6 Automated multi-cycle symbolic timing verification of microprocessor-based designs
Anurag P. Gupta, Daniel P. Siewiorek
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(140.84 KB) Additional Information: full citation, references, citings, index terms

7 High level and architectural synthesis: A symbolic approach for the combined solution of scheduling and allocation
Gianpiero Cabodi, Mihai Lazarescu, Luciano Lavagno, Sergio Nocco, Claudio Passerone, Stefano Quer
October 2002 **Proceedings of the 15th international symposium on System Synthesis**
Full text available: pdf(132.26 KB) Additional Information: full citation, abstract, references, index terms

Scheduling is widely recognized as a very important step in high-level synthesis. Nevertheless, it is usually done without taking into account the effects on the actual hardware implementation. This paper presents an efficient symbolic technique to concurrently integrate operation scheduling and resource allocation. The technique inherits all the features of "standard" BDD-based control dominated scheduling, including resource-constraining, speculation and pruning. In addition, it introduces an ...

Keywords: BDD, allocation, automata, high-level synthesis, scheduling

8 An RTL Methodology to Enable Low Overhead Combinational Testing
Subhrajit Bhattacharya, Sujit Dey, Bhaskar Sengupta
March 1997 **Proceedings of the 1997 European conference on Design and Test**
Full text available: pdf(872.56 KB) Publisher Site Additional Information: full citation, abstract

This paper introduces a low overhead test methodology, RT-SCAN, applicable to RT Level

designs. The methodology enables using combinational test patterns for testing the circuit, as done by traditional full-scan or parallel-scan schemes. However, by exploiting existing connectivity of registers through multiplexors and functional units, RT-SCAN reduces area overhead and test application times significantly compared to full-scan and parallel-scan schemes. Unlike most of the existing high-level te ...

Keywords: combinational circuits, RTL methodology, combinational testing, functional unit, RT-SCAN, multiplexor, register connectivity, application time, ATPG tool, area overhead, high-level test synthesis

9 Analysis of cyclic combinational circuits
Sharad Malik
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(770.89 KB) Additional Information: full citation, references, citings

10 Exploiting multi-cycle false paths in the performance optimization of sequential circuits
Pranav Ashar, Sujit Dey, Sharad Malik
November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(873.30 KB) Additional Information: full citation, references, citings, index terms

11 Hardware combining and scalability
Susan R. Dickey, Richard Kenner
June 1992 **Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(967.92 KB) Additional Information: full citation, references, citings, index terms

12 Session S3.1: architecture adaptation and synthesis: Cycle-time aware architecture synthesis of custom hardware accelerators
Mukund Sivaraman, Shail Aditya
October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(75.23 KB) Additional Information: full citation, abstract, references, index terms

We present the cycle-time aware architecture synthesis methodology used in PICO-NPA that automatically synthesizes minimal cost RT-level designs from high-level specifications to meet a given cycle-time. This allows subsequent physical synthesis to succeed on first pass with predictable performance. The core of the methodology is a static timing analysis engine that is used at multiple levels - program-level, architecture-level and RT-level - in order to identify, schedule and validate useful op ...

Keywords: clock frequency, delay analysis, embedded hardware architecture synthesis, high-level synthesis, operator chaining, target clock period, timing analysis, timing during scheduling

13 Timing abstraction: An implication-based method to detect multi-cycle paths in large sequential circuits
Hiroyuki Higuchi
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(247.01 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper proposes a fast multi-cycle path analysis method for large sequential circuits. It determines whether or not all the paths between every flip-flop pair are multi-cycle paths. The proposed method is based on ATPG techniques, especially on implication techniques, to utilize circuit structure and multi-cycle path condition directly. The method also checks whether or not the multi-cycle path may be invalidated by static hazards in combinational logic parts. Experimental results show that ...

Keywords: ATPG, implication, multi-cycle path, sequential circuits

14 On the combination of hardware and software concurrency extraction methods
Augustus K. Uht, Constantine D. Polychronopoulos, John F. Kolen
December 1987 **Proceedings of the 20th annual workshop on Microprogramming**
Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, references, citings

It has been shown that parallelism is a very promising alternative for enhancing computer performance. Parallelism, however, introduces much complexity to the programming effort. This has lead to the development of automatic concurrency extraction techniques. Prior work has demonstrated that static program restructuring via compiler based techniques provides a large degree of parallelism to the target machine. Purely hardware based extraction techniques (without software preprocessi ...

15 Analyzing cycle stealing on synchronous circuits with level-sensitive latches
I. Lin, J. A. Ludwig, K. Eng
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Full text available: pdf(685.55 KB) Additional Information: full citation, references, citings, index terms

16 Session I: transformation: Instruction combining for coalescing memory accesses using global code motion
Motohiro Kawahito, Hideaki Komatsu, Toshio Nakatani
June 2004 **Proceedings of the 2004 workshop on Memory system performance**
Full text available: pdf(195.53 KB) Additional Information: full citation, abstract, references, index terms

Instruction combining is an optimization to replace a sequence of instructions with a more efficient instruction yielding the same result in a fewer machine cycles. When we use it for *coalescing memory accesses*, we can reduce the memory traffic by combining narrow memory references with contiguous addresses into a wider reference for taking advantage of a wide-bus architecture. Coalescing memory accesses can improve performance for two reasons: one by reducing the additional cycles ...

Keywords: 64-bit architectures, IA-64, JIT compilers, Java, instruction combining, memory access coalescing

17 A performance bound analysis of multistage combining networks using a probabilistic model
Byung-ChangHo Kang, Gyungtto Lee, Richard Kain
June 1991 **Proceedings of the 5th international conference on Supercomputing**
Full text available: pdf(1.02 MB) Additional Information: full citation, references, citings, index terms

18 Effective Co-Verification of IEEE 802.11a MAC/PHY Combining Emulation and Simulation Technology
IL-Gu Lee, Seung-Beom Lee, Sin-Chong Park
April 2005 **Proceedings of the 38th annual Symposium on Simulation**

Full text available: pdf(358.72 KB) Additional Information: full citation, abstract

This work presents a system architecture and effective co-verification methodologies for the IEEE 802.11a Medium Access Control (MAC) layer/Physical (PHY) layer implementation. The architecture modeling includes hardware/software partitioning of a total system based on timing measurements from the C/C++ and Verilog design, and analysis of real-time requirements specified in the standard. The system is built on an evaluation platform that contains a Xilinx Virtex-II FPGA and an Altera Excalibur A ...

19 Understanding retiming through maximum average-weight cycles

Marios C. Papaefthymiou

June 1991 **Proceedings of the third annual ACM symposium on Parallel algorithms and architectures**

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20 Energy-per-cycle estimation at RTL

Subodh Gupta, Farid N. Najm

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**

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